the Examiner mailed May 2, 2003. Having addressed all objections and grounds of rejection, claims 1-20, being all the pending claims, are now deemed in condition for allowance. Entry of this amendment and reconsideration to that end is respectfully requested.

The Examiner has rejected claims 1, 6, and 16 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,276,848, issued to Gallagher et al (hereinafter referred to as "Gallagher"). This ground of rejection is respectfully traversed as based upon clearly erroneous findings of fact.

Specifically, the Examiner states at page 3, lines 2-4:

> ....a flush buffer responsively coupled to said store-in cache memory.....(i.e., store buffer in SCL 12 positioned between L1 and L3). (Emphasis added)

As admitted by the Examiner, the "store buffer in SCL 12 is positioned between L1 and L3". Gallagher states at column 1, line 56:

The L1 cache is a store-through cache....(emphasis added)

Therefore, Gallagher teaches coupling the "store buffer" to a "store-through" cache memory rather than the claimed "store-in" cache memory.

Furthermore, at page 9, the Examiner admits:

> Examiner agrees with Applicant that a store-through cache does not require a flush process as is well know (sic) in the art. (Emphasis added)

Therefore, the rejection of claims 1, 6, and 16 is respectfully traversed as based upon a clearly erroneous finding of fact.

The Examiner has simply repeated in his final office action, the same rejection as found in his initial office action. Applicants have made a similar argument with their previous submission. In response to Applicants' initial submission, the Examiner indicates at page 9 that Gallagher has a store-in L2 cache memory mentioned at column 1, lines 52-57. Applicants have admitted this in their previous submission. The Examiner goes on to allege, without adequate authority, that this L2 cache memory is coupled to a "flush buffer". However, in making his final rejection, the Examiner reads Applicants' claim limitations on Gallagher's L1 cache memory and "store buffer in SCL 12). Thus, the Examiner has disingenuously combined his clearly erroneous factual findings which support the claim rejections, with irrelevant and unsupportable findings which are unrelated to any claim rejections. It is deemed particularly unhelpful to the prosecution process to make unsupportable, yet irrelevant findings of fact.

In rejecting claim 7, the Examiner clearly erroneously states:

> As per claim 7, Gallagher discloses a flush buffer comprises a first flush buffer store and a second flush buffer store (i.e., buffers up to 8 stores (col. 3, lines 4-6).

The Examiner's citation reads:

> To assist this operation, a "store buffer" is present with the L1 data cache 18 which is capable of buffering up to 8 store operations.

As agreed to above, the L1 cache memory, being a store-through cache memory" does not have a "flush buffer". Furthermore, even if it did, it clearly has only a single "store buffer" with single input and output interfaces capable of buffering up to eight operations. This is readily distinguishable from Applicants' claimed invention which has multiple "flush buffers" having multiple input and output interfaces (i.e., each "flush buffer" has its own input and its own output).

Therefore, the rejection of claim 7, and all claims depending therefrom, is respectfully traversed as based upon a clearly erroneous finding of fact.

In rejecting claim 11, the Examiner makes the clearly erroneous finding:

> As per claim 11, Gallagher discloses the claimed invention as detailed above per claims 1 and 6. Gallagher further discloses selecting a particular location to a flush buffer (i.e., obsolete data)(col. 3, lines 1-3); transferring data from said particular location to a flush buffer (i.e., data stored in buffer for transfer)(col. 3, lines 1-6).

Gallagher actually states at column 3, lines 1-6:

> ....in L3 memory and, if the corresponding obsolete data is not present in the L1 caches 18, the data is not brought into and stored in the L1 caches. To assist this operation, a "store buffer" is present with

> the L1 data cache 18 which is capable of buffering up to 8 store operation.

Having established that the L1 cache memory is a store-through cache memory (col. 1, line 26), and having established that store-through cache memories do not "flush data" (as admitted by the Examiner), it is impossible to establish the claimed "selecting" and "transferring" steps using the Gallagher citation. The rejection of claim 11, and claims depending therefrom, is respectfully traversed as based upon clearly erroneous findings of fact.

In rejecting claims 2 and 12, the Examiner states:

> As per claims 2 and 12, Gallagher discloses the claimed invention as detailed above in the previous paragraphs. However, Gallagher does not specifically teach a tag memory indicating whether a particular memory location has been modified as recited in the claim.

It is true that Gallagher does not teach the claimed tag memory because the Examiner has relied upon the L1 store-through cache memory of Gallagher. Because there is no need to flush the store-through cache memory, there is no need to maintain a tag memory indicating whether a particular memory location has been modified. Therefore, one would not be motivated to make the alleged combination, because it would provide no benefit to Gallagher. The rejection of claims 2 and 12, and claims depending therefrom, is respectfully traversed as based upon

clearly erroneous findings of fact and lacking in motivation to make the alleged combination.

In rejecting claims 3 and 17, the Examiner admits:

> Gallagher does not specifically teach loading said flush buffer with data from said particular location within said store-in cache memory in response to said indication that said particular location has been modified as recited in the claim.

This statement is true, because the Examiner has not shown a "store-in" cache memory coupled to a "flush buffer". As a result of reading claims 1 and 16 on the L1, store-through, cache memory of Gallagher, the limitations of claims 3 and 17 have no meaning within the Gallagher system. The store-through L1 cache memory of Gallagher stores all data changes immediately by definition. Thus, there would certainly be no reason to combine any "indicating" structure from Jeddeloh. The rejection of claims 3 and 17 are respectfully traversed as based upon clearly erroneous findings of fact.

In rejecting claims 4 and 18, the Examiner states:

> As per claims 4 and 18, Gallagher discloses a flush buffer comprises a first flush buffer store and a second flush buffer store (i.e., buffers up to 8 stores)(col. 3, lines 4-6).

As explained above, Applicants claim two different flush buffers each having its own input and output interface (that is what makes them separate buffers rather than a single buffer). The rejection of claims 4 and 18, and the claims depending therefrom

is respectfully traversed as based upon clearly erroneous findings of fact.

In rejecting claims 5, 8, 10, and 19, the Examiner addresses "the concept of a temporary register" rather than the claim limitations. The claims are actually limited by "a temporary register" which routes data from the cache memory to one of the plurality of "flush buffers". Neither Gallagher nor Jeddeloh has this structure, because neither has a plurality of "flush buffers" each having its own input interface and output interface. The rejection of claims 5, 8, and 19, and any claims depending therefrom, is respectfully traversed as based upon clearly erroneous findings of fact.

Claims 9, 13, and 15 involve determining whether data needs to be rewritten during a flush operation. The L1 cache memory of Gallagher is a store-through cache memory which does not need a determination of whether to rewrite any particular data. It is always rewritten. Therefore, there can be no motivation to make the combination alleged by the Examiner. The rejection of claims 9, 13, and 15, and any claims depending therefrom, is respectfully traversed as based upon clearly erroneous findings of fact and failure to allege motivation, reasonable likelihood of success, and all claimed elements as required by MPEP 2143.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-20, being the only pending claims.

Respectfully submitted,

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By their attorney,

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